REMARKS

Reconsideration and withdrawal of the rejections set forth in the Office Action dated August 29, 2006 are respectfully requested. This communication is in response to the final Office Action dated August 29, 2006.

A. Claim 1, 5, 13, and 14 are not anticipated by Chang:

The Examiner argues that Chang (US Patent No. 5,969,383) discloses an NVM cell wherein the NVM cell contain two ONO stacks, each of these ONO stacks are capable of storing a single bit. The Examiner argues that this is exactly the same function used for nitride spacers 12 as shown in FIG. 1 of applicant's figures. The Applicant disagrees with the Examiner.

In fact, the multi-bit storing capability in the present invention is implemented by charges stored at multiple localized trapping sites especially in the nitride layer near its P-N junction. It should be noted, the present invention scheme is one cell having multi-bits instead of one cell one bit scheme disclosed by US Patent No. 5,969,383. The claimed invention is totally different from the cited prior art.

The scheme of the claimed invention and citation are briefly described below.

The present invention discloses one cell having two bits and multiple status schemes. The claimed invention includes one control gate having at least two bits charge trapping structure formed at the spaces of the control gate.

The Chang disclosed one cell having one bit and a two status scheme. Chang includes one spacer control gate having one bit charge trapping layer (the nitride of ONO). The only ONO layer having storage capability is the one under the spacer control gate.

It is well known that channel hot carriers are injected near the P-N junction during programming. For example, please refer to Lusky et al. (reference: *E. Lusky et al, "Investigation of channel hot electron injection by localized charge-trapping nonvolatile*

memory devices," IEEE Trans. Electron Devices, vol. 51, no. 3, pp. 444–451, Mar. 2004.) and the paper published by the inventor, Jeng et al. (reference: *Erik S. Jeng et al,"Investigation of Programming Charge Distribution in Nonoverlapped Implantation nMOSFETs", IEEE Trans. Electron Devices, vol. 53, no. 10, pp. 2517-2524, Oct. 2006*) Both papers report and confirm that the charge injection and trapping effects occur mainly near the P-N junction.

In other words, it is impossible for Chang's invention (US#5,969,383) to obtain multiple bits of storage since there is only one P-N junction (#22) formed under control gate (#32) and ONO (#28, #24 & #23). The other side of P-N junction (#22) is further away from the ONO under control gate, dielectric spacer (#34) and the control gate (#32). No memory storing capability is disclosed at the second P-N junction (#22) side of ONO layers based on Chang's description. In other words, the spacer trapping structure of the present invention is totally different from the silicon nitride layer 24 of Chang's. Instead of both ONO stacks, only one side's ONO, is capable of storing a bit since the other side's ONO cannot be controlled by the control gate (#32). However, the two-bits cell of the claimed invention is disclosed to be controlled by a single control gate without a select gate.

Moreover, the Examiner argues that Chang (US Patent No. 5,969,383) discloses that the selected gate "controls" the channel current, and, therefore, has a controlling function and may be construed as a "control gate". The Applicant disagrees with the Examiner.

Also in Chang's invention, a Control Gate (#32) and a Select Gate (#16) have been disclosed and defined in the specification of the Chang, simultaneously. The words, "Control" and "Select". However, both gates do differentiate each other in terms of their functionality in Chang's invention. The "Control Gate" is functioning to manipulate electrical fields to selectively perform Programming, Erasing or Reading operations. The term, "Control", is used for controlling different operations. On the other hand, the Select Gate functions as a selection switch to turn on the predetermined channel to be accessed for operations as mentioned above. The term, "Select", is used for selecting each operation bit. Makwana et al. also explain the Select Gate's function using Figure-3 in their

article that "...The select gate transistor is used to select or deselect floating gate transistors for programming or erasing..." (reference: *A Nonvolatile Memory Overview, by Jitu J. Makwana et al.*; website: http://aplawrence.com/Makwana/nonvolmem.html). It is well known that, in the Split Gate Memories, a relatively high voltage is applied to the Control Gate and a relatively low voltage is applied to the Select Gate to accomplish a programming operation. It is impossible, in Chang's invention, to electrically bias the Control Gate without biasing Select Gate for a successful programming operation. Neither structure elements nor their functionalities are found correspondingly equivalent between Chang's and the present inventions. Therefore, the quoted "control" is not only a label as the Examiner mentioned. The nonvolatile memory of the present invention is structurally different from the split–gate memory device of Chang's.

To summarize, the present invention provides a two-bit cell scheme in which one control gate controls two charge trapping spacers (two bits) 12. Thus, one cell of the claimed invention at least has the digital status of (0, 0), (1, 0), (0, 1) and (1, 1).

On the contrary, Chang's is a one-bit cell including a select gate and a control gate 32 formed on one side's ONO. Thus, one cell of the prior art can only achieve the status of digital 0 or digital 1. Chang uses one select gate 16 to select a one-bit cell rather than a two-bit cell. Accordingly, Chang fails to disclose the control gate structure with multiple spacer trapping structures of the present invention. Therefore, Chang's invention can not achieve the multiple-bit storage using multiple trapping sites in one cell.

According to the discussion of above, the independent Claim 1 is believed to overcome the rejection of novelty. Therefore, dependent Claims 5, 13, and 14 are overcome the rejection of novelty due to Claim 1 allowable.

B. Claims 2, 3, 6, 7, and 15 to 24 are patentable over Chang in view of Zheng:

As the argument set forth, Chang discloses a split–gate FET structure which is structurally different from the charge-trapping nonvolatile memory of the present invention. After carefully reviewing the citation of Zheng, Zheng also fails to disclose the control gate structure with spacer trapping structures of the present invention.

Moreover, no motivation can be found in the prior art to combine Chang and Zheng to achieve claim 1. Claim 1 can not be expected by the citations. Accordingly, Claim 1 is overcome the rejections of non-obviousness. Therefore, the dependency claims 2, 3, 6, 7, and 15 to 24 are patentable over Chang in view of Zheng, they should be overcome the rejections of non-obviousness.

C. Claims 4, 8, and 22 thru 24 are patentable over Chang in view of Kasuya and further in view of Zheng:

As the argument set forth, Chang discloses a split–gate FET structure which is structurally different from the charge-trapping nonvolatile memory of the present invention. After carefully reviewing the citation of Zheng and Kasuya, Zheng and Kasuya fail to disclose the control gate structure with spacer trapping structures of the present invention.

Moreover, no motivation can be found in the prior art to combine Chang, Kasuya and Zheng to achieve claim 1. Claim 1 can not be expected by the above citations. Accordingly, Claim 1 is overcome the rejections of non-obviousness. Therefore, the dependency claims 4, 8, and 22 thru 24 are patentable over Chang in view of Kasuya and further in view of Zheng, they should be overcome the rejections of non-obviousness.

Conclusion:

In view of the forgoing, claims 1-8, and 13-24 pending in the application comply with the requirements of patentability define over the applied art. A notice of allowance is, therefore, respectively requested.

Applicant believes no fees are due with this response. However, if any fee is due for consideration of this response, please charge our Deposit Account No. 50-0665, under Order No. 386998041US from which the undersigned is authorized to draw.

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Respectfully submitted,

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